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(54) Title: METHOD FOR HIGH YIELD RETICLE FORMATION

(57) Abstract: A system and method for optimizing the production of lithography reticles involves identifying "proximity effect halos" around tight tolerance features in an IC layout data file. Features and defects outside the halos will not have a significant effect on the printing of the tight tolerance features. During reticle formation, the tight tolerance features and associated halos can be carefully written and inspected to ensure accuracy while the other portions of the reticle can be written/inspected less stringently for efficiency. The halo width can be determined empirically or can be estimated by process modeling. If an electron beam tool is used to write the reticle, a small spot size can be used to expose the tight tolerance features and the halos, whereas a large spot size can be used to expose the remainder of the reticle. A reticle production system can include a computer to read an IC layout data file, identify tight tolerance features, and define proximity effect halos. Tight tolerance features can be individually selected or automatically flagged according to user specifications. A graphical user interface can be provided to enable user input and control. The reticle production system can be coupled to a remote IC layout database through a LAN or a WAN. The reticle production system can be coupled to directly send a reticle data file to a reticle-writing tool.

## 1 METHOD FOR HIGH YIELD RETICLE FORMATION

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3

4

5 FIELD OF THE INVENTION

6 The present invention relates to semiconductor  
7 device manufacturing and specifically to the efficient  
8 production of reticles for lithographic processes.

9

10 BACKGROUND OF THE INVENTION

11 Lithography masks (or "reticles") are key elements  
12 used in the production of integrated circuits (ICs). A  
13 portion of an IC layout data file (typically a  
14 representation of a physical layer, such as a metal layer  
15 or a polysilicon layer, of the final IC) is etched into a  
16 thin chrome layer formed over a glass plate to form a  
17 reticle. This reticle pattern ("reticle layout") is then  
18 exposed onto a layer of photosensitive resist on the  
19 surface of the wafer. Finally, the top surface of the  
20 wafer is chemically etched away in the areas not covered  
21 by the photoresist, thereby transferring the reticle  
22 layout onto the wafer. This transference process is  
23 known as lithography. The accuracy of the pattern formed  
24 on the wafer ("printed layout") significantly affects  
25 both process yield and the performance of the final IC.

26 The actual reticle formation process typically  
27 involves the steps of exposing the reticle pattern into a  
28 layer of resist on a blank reticle, developing the resist  
29 pattern (i.e. removing the exposed or unexposed portions  
30 of the resist layer), etching the resist pattern into the  
31 chrome layer of the reticle, inspecting the chrome  
32 pattern, and repairing any defects found in the chrome  
33 pattern.

1        While an optical projection (e.g. a laser beam  
2 scanner) system can be used to expose the reticle pattern  
3 into the resist layer, complex modern layouts are  
4 typically written by an electron beam scanner. Two main  
5 techniques are used in the exposing step of the electron  
6 beam writing process - raster scan and vector scan. In a  
7 raster scan system, the output of the scanner is moved in  
8 horizontal passes across the entire reticle and shifted  
9 an increment downwards after each pass, with the electron  
10 beam being applied to regions where the resist is to be  
11 exposed. The "spot size" of the electron beam can be set  
12 small to enable precise scanning of the reticle layout.  
13 However, a larger spot size is desirable to speed up the  
14 scanning process. Therefore, accuracy and throughput  
15 must be traded off against one another in conventional  
16 raster scan writing processes. An example of a raster  
17 scan system is the MEBES family of tools (models 4000,  
18 4500, 5000, 5500) from Etec Systems, Inc. (a subsidiary  
19 of Applied Materials Inc.).

20        In a vector scan system, the electron beam is moved  
21 directly to regions that are to be exposed. Most modern  
22 vector scan systems employ a shaped spot technique, in  
23 which the electron beam is formed into various primitive  
24 shapes (rectangles and triangles). The regions to be  
25 exposed are decomposed into primitives (rectangles and  
26 triangles), and each primitive is then exposed in a  
27 single shot by the electron beam, which is shaped to  
28 match the primitive being exposed. Vector scanning can  
29 be more efficient than raster scanning since the write  
30 tool does not have to scan the entire surface of the  
31 reticle. Therefore, a sparse layout will be written much  
32 faster on a vector scan system than a raster scan system.  
33 However, individually targeting the many features in a

1 dense, complex layout can make a vector scan system take  
2 longer to write the layout than a raster scan system.  
3 And as with raster scanning, beam spot size selection  
4 still must balance accuracy and throughput. Examples of  
5 vector scan systems include the JBX-6000FS from JEOL,  
6 Inc., the Vectorbeam from Leica Lithography Systems,  
7 Ltd., and the HL-800, HL-900, and HL-950 tools from  
8 Hitachi.

9 After the resist layer has been exposed, the resist  
10 pattern is developed. A negative resist is converted by  
11 the exposing radiation or electron beam into an insoluble  
12 state, and the developing process removes all the non-  
13 exposed portions of the resist layer. Exposure of a  
14 positive resist transforms the resist from an insoluble  
15 state into a soluble state, and the developing process  
16 then removes all the exposed portions of the resist  
17 layer. The chrome layer of the reticle is then etched  
18 through the pattern formed in the resist layer, after  
19 which the remaining resist is stripped from the reticle.

20 Next, an inspection tool checks to ensure that the  
21 IC layout has been properly written to the reticle. An  
22 optical image of the mask layout is checked against the  
23 original IC layout data, which may be modified to more  
24 accurately represent the expected output. Alternatively,  
25 for a reticle comprising multiple identical die layouts,  
26 the optical images of the individual die layouts can be  
27 compared against each other. Regardless of the specific  
28 comparison technique, the inspection sensitivity (i.e.  
29 the precision with which inspection is performed) is a  
30 key parameter of the inspection process. Because the  
31 entire reticle is typically inspected, a high inspection  
32 sensitivity can significantly increase the time required  
33 complete the process. A lower inspection sensitivity can

1 reduce the inspection time, but may miss defects or  
2 deviations in the reticle layout. Therefore,  
3 conventional inspection techniques are faced with a  
4 tradeoff between inspection sensitivity and efficiency.

5 Finally, defects and deviations detected during the  
6 inspection process are corrected. A laser tool (laser  
7 zapping or laser assisted deposition) is often used for  
8 rapid corrections, while a focused ion beam tool (ion  
9 milling or ion-assisted etch or deposition) provides more  
10 precise, yet slower, modifications.

11 Fig. 1 shows a technique proposed in an effort to  
12 address these mask making and inspection issues as  
13 described by Glasser et al., in PCT Patent Application  
14 No. PCT/US99/30240, filed December 17, 1999. Fig. 1  
15 shows a portion of an original IC layout comprising a  
16 diffusion region 110 and a polysilicon region 120. A  
17 critical region 130 of polysilicon region 120 is  
18 identified where polysilicon region 120 overlies  
19 diffusion region 110. This overlap of polysilicon region  
20 120 and diffusion region 110 represents a transistor gate  
21 to be formed in the final IC device. As a key feature of  
22 the final IC, the gate requires a high degree of  
23 precision to ensure proper performance of the transistor  
24 in the final IC device. However, other features of the  
25 IC layout may not require such a high degree of  
26 dimensional accuracy. For example, interconnects and  
27 contact pads can occupy a wider tolerance band than  
28 transistor gates without significantly affecting device  
29 performance. Consequently, by flagging critical regions  
30 such as region 130, special care can be directed towards  
31 those regions during mask making and/or inspection (e.g.  
32 very high inspection sensitivity). Less stringent  
33 standards (e.g. lower inspection sensitivity) can then be

1 applied to the remaining regions to improve throughput.  
2 Therefore, Glasser et al. attempts to efficiently form a  
3 high-yield reticle, i.e. a reticle that will produce  
4 critical features of the final IC accurately and  
5 consistently.

6       However, even though a particular portion of the  
7 original IC layout may correspond to a key feature in the  
8 final IC device, the actual creation of the key feature  
9 typically depends on much more than just the  
10 representation of that particular portion of the IC  
11 layout in a reticle. The mask-writing processes used to  
12 transfer the layout data to a reticle and the  
13 lithographic procedures used to print the reticle layout  
14 on a wafer are subject to "proximity effects", wherein  
15 the final dimensions of the features formed during the  
16 transference processes are affected by the presence or  
17 absence of neighboring features. For example, during  
18 optical lithography, the width of closely spaced lines  
19 may be different from the width of isolated lines, even  
20 if all the lines have the same width in the reticle.  
21 Also, the dimensions and regularity of a printed image  
22 can be affected by portions of adjacent features or even  
23 by nearby defects.

24       An example of a defect-induced proximity effect is  
25 shown in Figs. 2a and 2b. Fig. 2a shows a portion of a  
26 polysilicon layer reticle 200 that includes a reticle  
27 feature 210. Reticle feature 210 includes a critical  
28 region 211 (identified according to the technique of  
29 Glasser et al.; i.e. flagging the portion of reticle  
30 feature 210 that overlies a diffusion region in the  
31 original IC layout) that corresponds to a transistor gate  
32 to be formed in the final IC device. Special attention

1 can then be paid to critical region 211 during formation  
2 and inspection of reticle 200.

3       However, reticle 200 also includes a defect 212;  
4 i.e. an unintended marking in the opaque (chrome) layer  
5 of the reticle. Because regions outside of critical  
6 region 211 are written and inspected with less care than  
7 critical region 211 as taught by Glasser et al., defects  
8 like defect 212 are more likely to be created and be  
9 undetected in regions outside of critical region 211.  
10 Fig. 2b shows portion of a wafer 220 that includes a  
11 polysilicon feature 230 that might be produced from a  
12 lithography step using reticle 200. Polysilicon feature  
13 230 includes an actual gate profile 221 that deviates  
14 from a desired gate profile 240. Actual gate profile 221  
15 is created because of the proximity effects between  
16 reticle feature 210 and reticle defect 212 during  
17 lithography. Therefore, despite the identification of  
18 the critical region of the original IC layout and  
19 subsequent care focused on that critical region during  
20 both the reticle making and reticle inspecting steps, the  
21 final IC structure is undesirably deformed.

22       In addition, there may be purposely-added features  
23 outside of critical region 211 that play an important  
24 role in the formation of the final transistor gate. A  
25 technique known as optical proximity correction (OPC) has  
26 been developed in which features are introduced around  
27 (or modifications are made to) a critical layout feature  
28 to "precompensate" for predicted deformations during the  
29 lithography process. These OPC features and  
30 modifications must be reproduced with the same degree of  
31 accuracy as the actual layout feature of interest to  
32 ensure their proper effect. Similarly, original layout  
33 features adjacent to the critical feature must also be

1 accurately formed so that their effects can be reliably  
2 taken into account when incorporating OPC features.  
3 However, because the critical region only includes the  
4 critical feature itself, these influential external  
5 features will not receive the same degree of care in  
6 construction as the critical feature, often resulting in  
7 a less-than-desired final IC accuracy. Accordingly, it  
8 is desirable to provide a method for ensuring accurate  
9 formation and inspection of reticles that does not allow  
10 proximity effects to introduce unexpected deviations in  
11 the final IC features.

12

13 SUMMARY OF THE INVENTION

14 The invention provides a method for optimizing the  
15 production of lithography reticles by specifying  
16 "proximity effect halos" in an IC layout data file. The  
17 proximity effect halos represent the areas around tight  
18 tolerance layout features (i.e. layout features that  
19 correspond to features in the final IC that must be  
20 accurately formed) that can have an effect on the  
21 formation or inspection of those tight tolerance layout  
22 features. By applying a high degree of care to the  
23 proximity effect halos (as well as the tight tolerance  
24 layout features surrounded by the proximity effect halo  
25 regions) during reticle creation, a reticle capable of  
26 providing a high yield lithography process can be  
27 created. At the same time, once those areas requiring  
28 this enhanced scrutiny are identified, the remainder of  
29 the IC layout can be processed using less rigorous  
30 standards, thereby reducing the production time and cost  
31 of the reticle.

32 The width of the proximity effect halo is defined  
33 such that proximity effects on the enclosed tight



1 tolerance layout feature by features and/or defects  
2 outside the halo region are below a specified threshold  
3 level. In one embodiment of the invention, this width  
4 can be determined empirically, through measurements taken  
5 from the process(es) in which the IC layout will be used.  
6 In another embodiment of the invention, the width can be  
7 estimated by modeling the processes for making and using  
8 the reticle. For example, in an optical lithography  
9 process, proximity effects are proportional to the  
10 wavelength of the light used to expose the wafer, and are  
11 inversely proportional to the numerical aperture of the  
12 tool. Resist and etch effects can further add to the  
13 proximity effects, though such processes are less well  
14 characterized. Therefore, the width of the halo can be  
15 estimated by dividing wavelength by numerical aperture  
16 and multiplying the result by a constant to compensate  
17 for the resist/etch effects. Also, in an electron beam  
18 reticle writing operation, forward scattering and  
19 backscattering of the beam during the exposure process  
20 can introduce substantial proximity effects. Here too,  
21 modeling or data analysis could be used to determine an  
22 appropriate proximity effect halo width. In any case,  
23 the process in which proximity effects have the greatest  
24 range should control the width of the halo.

25       Once defined, the proximity effect halos can then be  
26 used to facilitate the production of high-yielding  
27 reticles. According to one embodiment of the invention,  
28 a raster scan tool can be used to write the reticle.  
29 Specifically, a small spot size is used to accurately  
30 expose the tight tolerance layout features and the  
31 proximity effect halos, whereas a larger spot size is  
32 used to efficiently expose the remainder of the reticle.  
33 According to another embodiment of the invention, a

1 vector scan tool can be used to write the reticle.  
2 Because tight tolerance layout features and associated  
3 proximity effect halos can be fractured individually,  
4 problems due to oddly shaped primitives can be minimized.

5 According to one embodiment of the invention, a  
6 reticle production system includes a computer and a  
7 graphical display, wherein the computer reads an IC  
8 layout data file, identifies tight tolerance layout  
9 features, and defines proximity effect halos around the  
10 tight tolerance layout features. According to an aspect  
11 of the invention, the key features can be manually  
12 identified (i.e. individually selected) by a user.  
13 According to another aspect of the invention, the user  
14 can specify specific layout features or configurations to  
15 be identified as key features. In one embodiment of the  
16 invention, a graphical user interface is provided to  
17 enable user input and control. In another embodiment of  
18 the invention, the reticle production system can be  
19 coupled to receive the IC layout data file from a remote  
20 database through a local area network or a wide area  
21 network. According to yet another embodiment of the  
22 invention, the reticle production system can be coupled  
23 to a reticle writing tool, which receives a reticle data  
24 file that includes the proximity effect halo data from  
25 the computer.

26

#### 27 BRIEF DESCRIPTION OF THE DRAWINGS

28 Fig. 1 shows a sample portion of an IC layout having  
29 a critical region flagged in accordance with the prior  
30 art.

31 Figs. 2a and 2b illustrate a proximity effect caused  
32 by a reticle defect.

1        Fig. 3 shows a sample proximity effect halo in  
2        accordance with the invention.

3        Fig. 4a shows a flow diagram of a reticle creation  
4        process in accordance with an embodiment of the  
5        invention.

6        Fig. 4b shows a flow diagram of a reticle writing  
7        operation using a raster scan tool in accordance with an  
8        embodiment of the invention.

9        Fig. 4c shows a flow diagram of a reticle writing  
10       operation using a vector scan tool in accordance with an  
11       embodiment of the invention.

12       Fig. 5 illustrates a raster scan reticle writing  
13       process in accordance with an embodiment of the  
14       invention.

15       Fig. 6 shows a diagram of a reticle layout  
16       processing system in accordance with an embodiment of the  
17       present invention.

18

19       DETAILED DESCRIPTION OF THE DRAWINGS

20       Fig. 3 provides an example of a "tight tolerance  
21       feature" that could require special attention during  
22       reticle writing to ensure proper device formation during  
23       lithography. Fig. 3 shows sample layout features 310 and  
24       320 that can commonly be found in a conventional IC  
25       layout design. As depicted in Fig. 3, layout feature 320  
26       represents a feature to be formed in a polysilicon layer  
27       of an IC, over a diffusion region represented by layout  
28       feature 310. Layout features 310 and 320 therefore  
29       designate a transistor to be formed in the IC, the gate  
30       of the transistor being defined where layout feature 320  
31       overlies layout feature 310. Accordingly, layout feature  
32       320 includes a tight tolerance feature 321 that  
33       corresponds to this overlap region. Tight tolerance

1 feature 321 must be accurately formed in the final IC  
2 since the gate of a transistor is so critical to device  
3 performance.

4

5 Proximity Effect Halo

6 To ensure this accurate formation of tight tolerance  
7 feature 321, a proximity effect halo 331 is designated  
8 around tight tolerance feature 321. Proximity effect  
9 halo 331 extends a distance  $d$  from each edge of tight  
10 tolerance feature 321. Distance  $d$  represents a  
11 "proximity effect range" and is selected so that any  
12 features outside proximity effect halo 331 will have a  
13 negligible effect on tight tolerance feature 321 during  
14 reticle formation or wafer patterning. Note that the  
15 outer perimeter of proximity effect halo 331 could have  
16 rounded corners to maintain a completely constant spacing  
17 from tight tolerance feature 321. However, the square  
18 corners shown are simpler to define and process, and do  
19 not occupy a significantly larger area of the layout.

20 Together, tight tolerance feature 321 and proximity  
21 effect halo 331 form a tight tolerance zone 330.  
22 Enhanced care can be directed towards tight tolerance  
23 zone 330 during reticle formation to ensure accurate  
24 patterning, while standard care can be applied to the  
25 less dimension-critical regions outside of tight  
26 tolerance zone 330 to improve throughput.

27

28 Proximity Effect Range

29 As described previously, distance  $d$  is selected such  
30 that any feature or potential defect that could have a  
31 significant proximity effect on tight tolerance feature  
32 321 will be included in proximity effect halo 331.  
33 Proximity effect halo 331 would typically not incorporate

1 all features/defects that could introduce any amount of  
2 proximity effect during the printing of tight tolerance  
3 feature 321. Such a comprehensive approach would  
4 generally be undesirable, because distortions in IC  
5 elements below a certain level would not provide much  
6 benefit to IC performance, but would require an  
7 excessively large proximity effect halo. This approach,  
8 in turn, would tend to negate the efficiency benefits  
9 derived from applying enhanced care to only those tight  
10 tolerance zones as the tight tolerance zones would then  
11 be occupying most of the pattern area. Therefore, the  
12 proximity effect range should be selected to encompass  
13 only those features/potential defects that could have a  
14 proximity effect above a certain threshold on the tight  
15 tolerance feature.

16 Proximity effects show up during both the wafer  
17 patterning process (lithography) and the actual reticle  
18 formation processes. Accordingly, the proximity effect  
19 range could be derived from the process having the  
20 greatest sensitivity to proximity effects, i.e. the  
21 process in which threshold proximity effects arise at the  
22 greatest distance.

23

#### 24 Wafer Patterning

25 The proximity effect range for wafer patterning is a  
26 function of both diffraction effects and process effects.  
27 A reticle layout is exposed onto a wafer by a radiation  
28 (light) source of a lithography tool. As the exposing  
29 light passes through the fine transparent regions of the  
30 reticle, diffraction effects between adjacent features  
31 lead to distortions in the patterns projected onto the  
32 resist layer of the wafer. These diffraction effects are  
33 a function of the lithography tool characteristics,

1 including numerical aperture (NA), wavelength of the  
2 exposing radiation, and coherence of the exposing  
3 radiation, which is in turn a function of the type of  
4 illumination used (i.e. on-axis or off-axis  
5 illumination).

6 Further distortions can occur as the projected image  
7 is subsequently transferred into the wafer surface.  
8 These additional deformations are due to process effects  
9 that take place during the physical processing of the  
10 wafer. For example, because the intensity of the  
11 exposing light does not immediately drop to zero at the  
12 edges of layout features, but rather decreases at some  
13 gradient, the edges of those layout features are  
14 partially developed. Depending on the sharpness of the  
15 edge intensity gradient and the sensitivity of the  
16 resist, this partial edge developing can introduce  
17 additional deviations from the desired feature outline.  
18 Similarly, when the wafer is dry etched to transfer the  
19 pattern in the resist to the wafer surface, the resist  
20 layer that remains can be attacked by the etchant ions,  
21 thereby leading to further defects. In addition, the  
22 high temperatures used in the etch process can cause flow  
23 and distortion of the resist pattern.

24 According to one aspect of the invention, the wafer  
25 patterning proximity effect range can be derived through  
26 empirical data. Because of the complex interactions  
27 between the diffraction and process effects as described  
28 above, an empirical approach can provide a  
29 straightforward means for determining an appropriate  
30 proximity effect range. The empirical result can be  
31 derived from actual data from the lithography process.  
32 According to another aspect of the invention, a formula  
33 or model can be used to provide an estimate for the

1 proximity effect range. For example, it is known that  
2 diffraction effects are proportional to wavelength over  
3 numerical aperture. Therefore, a formula for the  
4 approximate proximity effect range could be as follows:

$$5 \quad d = k \cdot \lambda / NA \quad [1]$$

7  
8 where d is the proximity effect range,  $\lambda$  is the  
9 wavelength of the exposing radiation, NA is the numerical  
10 aperture of the tool, and k is a correction constant that  
11 adjusts for the coherence of the exposing radiation and  
12 the resist and dry etch effects. A typical correction  
13 constant for a 365nm wavelength, 0.6 NA process could be  
14  $k = 2.5$ , which would produce a proximity effect range  $d =$   
15  $1.5\mu\text{m}$ . Changing the wavelength to 248nm would then  
16 result in a proximity effect range  $d = 1\mu\text{m}$ . When using a  
17 formula-based approach, a "buffer offset" can be added to  
18 the calculated proximity effect range to ensure full  
19 coverage of the required area.

20

#### 21 Reticle Writing/Inspecting

22 As indicated previously, it is possible that  
23 portions of the reticle formation process could have even  
24 more sensitivity to proximity effects than the  
25 lithography process. In such a case, the proximity  
26 effect range would be based on the affected step(s)  
27 within the reticle formation process. Typically, the  
28 reticle writing operation can have a high susceptibility  
29 to proximity effects. The two main techniques used to  
30 write IC layout data to a reticle are optical writing and  
31 electron beam (e-beam) writing. In an optical system, a  
32 light source is used to expose the IC layout pattern onto  
33 the reticle. Accordingly, the proximity effect range for

1 such a process could be affected by diffraction of the  
2 light source. As with the wafer patterning procedure,  
3 the proximity effect range of an optical reticle writing  
4 system could be either determined through empirical data,  
5 or calculated using known optical formulae. However,  
6 because the reticle is typically written at 4 to 5 times  
7 the size of the final printed (wafer) image, the  
8 diffraction interactions would typically not be as great  
9 as those seen in a lithography step involving the same  
10 layout. Examples of optical reticle writing tools  
11 include the Core2564, Alta3000, Alta3500, and Alta3700  
12 from ETEC Systems, Inc., and the Omega6000 tool from  
13 Micronic Laser Systems.

14 In an e-beam system, a focused electron beam (or a  
15 shaped beam for vector scan tools) is used to write  
16 specified patterns into the resist layer on the reticle  
17 surface. Because the beam is not being projected through  
18 a pattern, diffraction effects are minimized. However,  
19 as the electrons penetrate the resist, they can  
20 experience directional deflection as they pass through  
21 the resist layer (forward scattering) and when they enter  
22 the reticle surface (backscattering). These scattering  
23 effects "spread" the area exposed by the e-beam, and can  
24 therefore introduce significant proximity effects.

25 Scattering effects are exacerbated as e-beam power  
26 is increased to write more complex layout patterns. For  
27 example, a 10keV e-beam tool may introduce scattering  
28 effects on the order of  $2\mu\text{m}$  for a 4-5X reticle. This  
29 translates into a 0.4-0.5 $\mu\text{m}$  reticle proximity effect  
30 range (at the original layout size, i.e. 1X), which would  
31 typically be less than the wafer proximity effect range.  
32 However, a 50keV e-beam tool can cause scattering effects  
33 on the order of  $15\mu\text{m}$  for a 4-5X reticle. These figures



1 translate into a 3-3.75 $\mu$ m reticle proximity effect range  
2 (1X), which can be significantly larger than the wafer  
3 proximity effect range. While modeling or calculation of  
4 the scattering effects could be possible, the complexity  
5 and probabilistic nature of the interactions could make  
6 such calculations difficult. Using empirical data to  
7 derive a proximity effect range for an e-beam tool could  
8 provide a more efficient and accurate value. Examples of  
9 e-beam reticle writing tools include the MEBES tools from  
10 ETEC Systems, Inc., the HL800, HL900, and HL950 tools  
11 from Hitachi, the JBX-6000FS tool from JEOL, Inc., and  
12 the Vectorbeam tool from Leica Lithography Systems, Ltd.

13 Finally, proximity effects also affect the  
14 inspection of the patterned reticle as an optical image  
15 from the completed reticle is typically used in the  
16 inspection process. Because this optical process is  
17 typically performed at a 4-5X magnification, inspection  
18 proximity effects should be much less pronounced than  
19 wafer proximity effects. However, as with lithography or  
20 reticle writing, an inspection proximity effect range  
21 could be determined either empirically or theoretically,  
22 and if larger than the lithography or reticle writing  
23 ranges, could be used to define the overall proximity  
24 effect range. Examples of reticle inspection tools  
25 include the KLA200 and KLA300 series tools from KLA-  
26 Tencor, Inc., the Orbot RT800, RT8000, and the ARIS-i  
27 tools from Applied Materials, Inc., and the 9MD series  
28 tools from Lasertech Corp.

29

### 30 Reticle Production

31 Once the proximity effect range has been defined, it  
32 can be used in the creation of a reticle. Fig. 4a shows  
33 a flow diagram of a reticle writing method in accordance

1 with one embodiment of the invention. In step 410, an IC  
2 layout data file is read and tight tolerance features are  
3 identified. The tight tolerance features can be  
4 identified manually by a user selecting individual  
5 elements of the layout requiring a high degree of  
6 transference precision. Alternatively, in another  
7 embodiment, automated means could be used to detect tight  
8 tolerance features, for example by detecting specific  
9 layout elements (e.g. transistor gates or capacitors) or  
10 specific layout feature configurations (e.g. a single-  
11 layer configuration, such as an isolated line, or a  
12 multi-layer configuration, such as a polysilicon feature  
13 over diffusion region). In another embodiment of the  
14 invention, the tight tolerance features can be  
15 automatically detected by scanning for OPC features (such  
16 as assist features or serifs), and then flagging the  
17 layout features associated with those OPC features.  
18 According to an embodiment of the invention, a design  
19 rule checker (DRC) tool could be used to detect tight  
20 tolerance features. For example, a gate region such as  
21 tight tolerance feature 321 in Fig. 3 can be identified  
22 by instructing a DRC tool to perform a Boolean AND  
23 operation between the polysilicon layer and the diffusion  
24 layer. Examples of DRC tools include ASSURA from Cadence  
25 Design Systems, Calibre from Mentor Graphics Corp., and  
26 Hercules from Avant!.

27 After identification of the tight tolerance  
28 features, proximity effect halos for each of the features  
29 are defined in step 420. According to one embodiment of  
30 the present invention, a proximity effect halo could be  
31 assigned as each tight tolerance feature is identified.  
32 As described previously, each proximity effect halo is  
33 formed by delineating a width equal to the proximity

1 effect range from each edge of the associated tight  
2 tolerance feature. Each tight tolerance feature and  
3 associated proximity effect halo can be combined to form  
4 a tight tolerance zone. A reticle data file, including  
5 the proximity effect halo/tight tolerance zone data, can  
6 then be passed to a reticle writing tool.

7 The reticle is written in step 430, wherein the  
8 tight tolerance features and regions within the proximity  
9 effect halos are written with greater care than the rest  
10 of the IC layout. As noted previously, the blank (i.e.  
11 unpatterned) reticle can be written either optically or  
12 by an e-beam. While an optical tool typically exposes  
13 the reticle in a single step, e-beam tools require  
14 multiple steps to most effectively make use of the  
15 identified tight tolerance zones. Fig. 4b shows a flow  
16 diagram of a method for writing a reticle using a raster  
17 scan e-beam tool according to an embodiment of the  
18 invention. First, the e-beam is set to a small (high-  
19 precision) spot size in step 431b. The tight tolerance  
20 zones are then rastered in step 432b. Next, the e-beam  
21 is set to a large (high-speed) spot size in step 433b.  
22 Finally, the remainder of the reticle (non-tight  
23 tolerance zones) is rastered in step 434b, thereby  
24 completing the exposure process. According to another  
25 embodiment of the invention, the tight tolerance zones  
26 are rastered after the high-speed scan has exposed the  
27 non-tight tolerance regions.

28 An example of an e-beam raster scan process as  
29 described in Fig. 4b is depicted in Fig. 5. Fig. 5 shows  
30 a portion of an IC layout, comprising a layout feature  
31 520 that includes a tight tolerance feature 521. A  
32 proximity effect halo 531 has been identified around  
33 tight tolerance feature 521 to form a tight tolerance

1 zone 530. An e-beam having a small spot size S1 is used  
2 to scan tight tolerance zone 530 along a path P1 to  
3 ensure accurate transfer of tight tolerance feature 521  
4 and any adjacent areas that could contain features within  
5 the proximity effect range of feature 521. An e-beam  
6 having a large spot size S2 is used to scan the remaining  
7 portions of the IC layout along a path P2 to minimize the  
8 total time required for rastering.

9       Instead of using a raster scan method, an e-beam  
10 tool could be set up to perform vector scanning. Fig. 4c  
11 shows a flow diagram of a method for writing a reticle  
12 using a vector scan e-beam tool according to one  
13 embodiment of the invention. In a vector scan tool, the  
14 e-beam is moved directly to regions of the reticle to be  
15 exposed. Each of those regions is fractured into  
16 primitive shapes, with each of the primitive shapes being  
17 exposed by the similarly shaped e-beam in a single shot.  
18 If any of the primitive shapes are very narrow (i.e. very  
19 low or very high aspect ratio), the accuracy and quality  
20 of the exposure process can be degraded. In conventional  
21 vector scan systems, undesirable primitives are difficult  
22 to avoid because such a large amount of data is being  
23 fractured. However, in step 431c, just the tight  
24 tolerance zones are fractured, thereby enabling greater  
25 control over the fracturing process to avoid excessively  
26 narrow primitives. An example of a fracturing tool is  
27 the CATS tool from Transcription Enterprise Inc., a  
28 subsidiary of Numerical Technologies, Inc.

29       Because such a limited area is being fractured, the  
30 final primitives can be readily adjusted to optimize  
31 their shapes. According to an aspect of the invention, a  
32 tight tolerance zone including a transistor gate could be  
33 fractured for a negative resist process such that the

1 gate (i.e. the tight tolerance feature) is a single  
2 primitive. The gate could then be exposed in a single  
3 shot for enhanced accuracy. According to another aspect  
4 of the invention, a tight tolerance zone including a  
5 transistor gate could be fractured for a positive resist  
6 process such that the proximity effect halo is decomposed  
7 into equal-sized primitives. Since the complement of  
8 layout features is typically being exposed in a positive  
9 resist process, the use of consistent primitives enhances  
10 the regularity of the actual (unexposed) feature.

11 After the fracturing step of 431c, each primitive is  
12 exposed in a single shot by a correspondingly shaped beam  
13 in step 432c. In step 433c, the remaining data is  
14 fractured, and in step 434c, those remaining primitives  
15 are exposed. According to another embodiment of the  
16 invention, the fracturing of the non-tight tolerance  
17 portions of the layout (step 433c) is performed  
18 immediately after the fracturing of the tight tolerance  
19 zones (step 431c), after which all the primitives are  
20 exposed by the electron beam.

21 Returning to Fig. 4a, once the reticle has been  
22 written, the exposed pattern is developed in the resist  
23 and is subsequently etched into the chrome layer of the  
24 reticle in step 440. The finished reticle is then  
25 inspected in step 450. According to one embodiment of  
26 the invention, the inspection process could be set up to  
27 apply high inspection sensitivity to the regions of the  
28 reticle corresponding to tight tolerance zones while  
29 applying standard (i.e. less stringent) inspection  
30 sensitivity to the remainder of the reticle. In this  
31 manner, the truly key portions of the reticle are  
32 carefully checked to ensure a high yield reticle, whereas  
33 the less crucial portions of the reticle are inspected at

1 a more appropriate level, to allow a faster overall  
2 inspection process.

3 Finally, any defects or deviations from the desired  
4 pattern detected in step 450 are repaired in step 460.  
5 According to an embodiment of the invention, a focused  
6 ion beam (FIB) tool could be used to perform precise  
7 repairs within the tight tolerance zones, while a laser  
8 tool could be used to more quickly fix defects in less  
9 sensitive regions.

10

#### 11 High Yield Reticle System

12 Fig. 6 shows a diagram of a proximity effect halo  
13 processing system 610 according to one embodiment of the  
14 invention. System 610 comprises at least one computer  
15 614 and a graphical display 612. Computer 614 could  
16 comprise a personal computer (PC) running Microsoft™  
17 software and/or a workstation such as a Sun™ workstation  
18 running the Solaris™ operating system. Graphical display  
19 612 allows a user to monitor and control the IC layout  
20 processing operations being performed by system 610. For  
21 example, graphical display 612 could provide a graphical  
22 user interface (GUI) through which a user could input  
23 proximity effect range specifications or tight tolerance  
24 feature settings.

25 Computer 614 typically includes a processing module  
26 to identify tight tolerance features of an IC layout and  
27 define proximity effect halos, as described in steps 410  
28 and 420, respectively, of the flow diagram shown in Fig.  
29 4a. According to an aspect of the invention, the  
30 processing module can be implemented in software.  
31 According to another aspect of the invention, the  
32 processing module can be a hardware element, such as a  
33 ROM (random operating memory) chipset.

1        Fig. 6 also shows an IC layout database 620, a  
2        reticle writing tool 630, an inspection tool 640, and a  
3        repair tool 650, all of which may be located physically  
4        apart from system 610. IC layout database 620 can  
5        provide a centralized storage area for IC layout data  
6        files. Alternatively, the IC layout data files could be  
7        stored locally in computer 614, or even in reticle  
8        writing tool 630. According to an aspect of the  
9        invention, computer 614 may access IC layout database 620  
10       for files to be processed for reticle writing through a  
11       local area network (LAN). In another embodiment of the  
12       invention, IC layout database 620 may be accessed though  
13       a wide area network (WAN), such as the Internet. System  
14       610 sends the reticle data file (including proximity  
15       effect halo information) to reticle writing tool 630,  
16       which patterns the reticle and sends it to inspection  
17       tool 640. Inspection tool 640 is also provided with the  
18       modified layout data file so that the inspection process  
19       can be optimized. Finally, the inspected reticle and its  
20       associated defect data are provided to repair tool 650,  
21       along with the modified layout data file. Repair tool  
22       650 can then perform defect repair based on the tight  
23       tolerance zones defined in the modified layout data file.  
24       According to an aspect of the invention, repair tool 650  
25       could be set to perform high-precision repairs on defects  
26       within the tight tolerance zones and low-precision  
27       repairs on all other defects. According to another  
28       embodiment of the invention, repair tool 650 could be  
29       replaced with two different repair tools, a focused ion  
30       beam tool for tight tolerance zone defects, and a laser  
31       tool for all other defects. As with IC layout database  
32       620, reticle writing tool 630, inspection tool 640, and  
33       repair tool 650 may be connected to computer 614 through

1 a LAN or a WAN, or may communicate through a direct (i.e.  
2 non-networked) connection.

3

4 Conclusion

5 Thus, the present invention ensures efficient  
6 production of high yield reticles. Specifically, by  
7 identifying IC layout features requiring a high degree of  
8 accuracy, and then identifying the adjacent regions that  
9 could affect the formation of those features, the  
10 portions of a reticle that strongly affect the  
11 performance of the final IC can be precisely formed and  
12 inspected. At the same time, less stringent controls can  
13 be placed on the formation and inspection of the  
14 remaining areas, thereby minimizing the time required to  
15 form the finished reticle.

16 The above disclosure is not intended to be limiting.  
17 Numerous modifications and variations of the invention  
18 will be apparent to one of ordinary skill in the art.  
19 For example, while tight tolerance feature 321 is shown  
20 as representing a transistor gate in Fig. 3, any layout  
21 feature(s) could be specified as the tight tolerance  
22 feature(s). Similarly, while tight tolerance feature 321  
23 and tight tolerance zone 330 in Fig. 3 are shown as  
24 having substantially rectangular outlines, a tight  
25 tolerance feature could have any outline and its  
26 associated tight tolerance zone would simply parallel  
27 that outline. Also, while system 610 in Fig. 6 is  
28 depicted as a computer 614, system 610 could also be a  
29 client for a remote server that does the actual layout  
30 processing. In addition, while system 610 is shown as  
31 being separate from reticle writing tool 630, system 610  
32 could be incorporated directly in tool 630. Therefore,  
33 the invention is limited only by the following claims.



1    CLAIMS

2

3            1.    A method for creating a lithography reticle  
4            from an integrated circuit (IC) layout data file, the  
5            method comprising the steps of:

6                    identifying a plurality of layout features in  
7            the IC layout data file; and

8                    defining a plurality of halo regions, each of  
9            the plurality of halo regions having an inner  
10           perimeter and an outer perimeter, the inner  
11           perimeter of each of the plurality of halo regions  
12           being defined by the outer perimeter of a  
13           corresponding one of the plurality of layout  
14           features, and the inner perimeter and the outer  
15           perimeter of each of the plurality of halo regions  
16           being substantially parallel.

17

18           2.    The method of Claim 1, wherein each of the  
19           plurality of halo regions has a substantially constant  
20           width.

21

22           3.    The method of Claim 1, wherein the step of  
23           identifying the plurality of layout features comprises  
24           manually selecting features within the IC layout data  
25           file.

26

27           4.    The method of Claim 1, wherein the step of  
28           identifying the plurality of layout features comprises  
29           the steps of:

30                    specifying a layout element;

31                    scanning the IC layout data file; and

32                    flagging locations in the IC layout data file  
33                    matching the layout element.

1

2           5.    The method of Claim 4, wherein the layout  
3 element comprises a transistor gate.

4

5           6.    The method of Claim 4, wherein the layout  
6 element comprises a capacitor.

7

8           7.    The method of Claim 1, wherein the step of  
9 identifying the plurality of layout features comprises  
10 the steps of:

11               specifying a plurality of layout elements;  
12               scanning the IC layout data file; and  
13               flagging locations in the IC layout data file  
14           matching one of the plurality of layout features.

15

16           8.    The method of Claim 1, wherein the IC layout  
17 data file comprises a plurality of layer layouts, each of  
18 the layer layouts corresponding to a single process layer  
19 in a completed IC, the step of identifying the plurality  
20 of layout features comprising the steps of:

21               specifying a layout feature configuration;  
22               scanning a first one of the plurality of layer  
23           layouts; and  
24               flagging locations in the first one of the  
25           plurality of layer layouts matching the layout  
26           feature configuration.

27

28           9.    The method of Claim 8, wherein the layout  
29 feature configuration comprises a single-layer  
30 configuration.

31

1           10. The method of Claim 8, wherein the layout  
2 feature configuration comprises a multi-layer  
3 configuration.  
4

5           11. The method of Claim 10, wherein the first one  
6 of the plurality of layer layouts corresponds to a  
7 polysilicon layer of the completed IC, and wherein the  
8 multi-layer configuration comprises a feature in the  
9 first one of the plurality of layer layouts formed over  
10 any feature in a second one of the plurality of layer  
11 layouts, the second one of the plurality of layer layouts  
12 corresponding to a diffusion layer of the completed IC.  
13

14           12. The method of Claim 1, wherein the step of  
15 identifying the plurality of layout features comprises  
16 the steps of:

17                 scanning the IC layout data file;  
18                 identifying optical proximity correction (OPC)  
19 features; and  
20                 flagging locations in the IC layout data file  
21 associated with the OPC features.  
22

23           13. The method of Claim 2, wherein the step of  
24 defining a plurality of halo regions comprises the steps  
25 of:

26                 defining the inner perimeter of each of the  
27 plurality of halo regions;  
28                 specifying a parallel line at the substantially  
29 constant width from each edge of the inner perimeter  
30 of each of the plurality of halo regions; and  
31                 connecting the parallel lines around each inner  
32 perimeter of each of the plurality of halo regions.  
33

1        14. The method of Claim 13, wherein the  
2 substantially constant width is defined to be a distance  
3 at which proximity effects in a lithography process using  
4 the lithography reticle are less than a specified  
5 threshold level.

6  
7        15. The method of Claim 13, wherein the  
8 substantially constant width is defined to be a distance  
9 at which proximity effects in a reticle formation process  
10 for the lithography reticle are less than a specified  
11 threshold level.

12  
13        16. The method of Claim 13, wherein the  
14 substantially constant width is defined to be the greater  
15 of a first distance, at which proximity effects in a  
16 lithography process using the lithography reticle are  
17 less than a specified threshold level, and a second  
18 distance, at which proximity effects in a reticle  
19 formation process for the lithography reticle are less  
20 than the specified threshold level.

21  
22        17. The method of Claim 14, wherein the distance is  
23 determined empirically using measured proximity effect  
24 data.

25  
26        18. The method of Claim 14, wherein the lithography  
27 reticle is used in a lithography process using an  
28 exposing radiation of a substantially constant wavelength  
29 and having a substantially constant numerical aperture  
30 (NA), the distance being estimated by dividing the  
31 substantially constant wavelength by the NA and  
32 multiplying the result by a constant correction factor to  
33 compensate for resist and etch effects.

1  
2       19. The method of Claim 18, wherein the distance is  
3 approximately equal to 1.5 microns when the substantially  
4 constant wavelength is 365 nm and the NA is 0.6.

5  
6       20. The method of Claim 18, wherein the distance is  
7 approximately equal to 1.0 microns when the substantially  
8 constant wavelength is 248 nm and the NA is 0.6.

9  
10       21. The method of Claim 15, wherein the distance is  
11 between 3.0 $\mu$ m and 3.75 $\mu$ m for a 50keV electron beam  
12 reticle writing process.

13  
14       22. The method of Claim 1, further comprising the  
15 steps of:  
16               writing the IC layout data file to the  
17 lithography reticle;  
18               inspecting the lithography reticle; and  
19               repairing the lithography reticle.

20  
21       23. The method of Claim 22, wherein the step of  
22 writing is performed using a raster scan tool, the raster  
23 scan tool having a first beam spot size and a second beam  
24 spot size, the first beam spot size being smaller than  
25 the second beam spot size, wherein the step of writing  
26 comprises the steps of:

27               rastering the portions of the lithography  
28 reticle corresponding to the plurality of layout  
29 features and the plurality of halo regions using the  
30 first beam spot size; and  
31               rastering the remainder of the lithography  
32 reticle using the second beam spot size.

33

1           24. The method of Claim 22, wherein the step of  
2 writing is performed using a vector scan tool, the vector  
3 scan tool being capable of generating an adjustable  
4 electron beam, wherein the step of writing comprises the  
5 steps of:

6           combining each of the plurality of halo regions  
7 with the corresponding one of the plurality of  
8 layout features to define a plurality of tight  
9 tolerance zones;

10          fracturing each of the plurality of tight  
11 tolerance zones into a first plurality of  
12 primitives, wherein each of the first plurality of  
13 primitives comprising one of a plurality of shapes  
14 that can be formed by the adjustable electron beam;

15          fracturing the remainder of the IC layout data  
16 file into a second plurality of primitives, each of  
17 the second plurality of primitives comprising one of  
18 the plurality of shapes that can be formed by the  
19 adjustable electron beam;

20          exposing each of the first plurality of  
21 primitives;

22          and

23          exposing each of the second plurality of  
24 primitives.

25

26          25. The method of Claim 24, wherein each of the  
27 first plurality of primitives has a width greater than a  
28 base width, the base width being sized to be larger than  
29 the minimum beam width of the vector scan tool.

30

31          26. The method of Claim 24, wherein a negative  
32 resist process is being used, the step of fracturing each  
33 of the plurality of tight tolerance zones comprising the

1 step of forming a single primitive around each of the  
2 plurality of layout features.

3

4 27. The method of Claim 24, wherein a positive  
5 resist process is being used, the step of fracturing each  
6 of the plurality of tight tolerance zones comprising  
7 forming a set of primitives of substantially similar  
8 shape around each of the plurality of layout features.

9

10 28. The method of Claim 22, wherein the step of  
11 inspecting comprises the steps of:

12 inspecting portions of the lithography reticle  
13 corresponding to the plurality of halo regions and  
14 the plurality of layout features according to a  
15 first level of scrutiny; and

16 inspecting portions of the lithography reticle  
17 not corresponding to the plurality of halo regions  
18 and the plurality of layout features according to a  
19 second level of scrutiny, the first level of  
20 scrutiny being more rigorous than the second level  
21 of scrutiny.

22

23 29. The method of Claim 22, wherein the step of  
24 inspecting detects a first plurality of defects within  
25 the plurality of halo regions and the plurality of layout  
26 features and a second plurality of defects not within the  
27 plurality of halo regions and the plurality of layout  
28 features, the step of repairing comprising the steps of:

29 repairing the first plurality of defects using  
30 a first repair process; and

31 repairing the second plurality of defects using  
32 a second repair process, wherein the first repair  
33 process is more accurate than the second repair

1 process, and wherein the second repair process is  
2 faster than the first repair process.

3  
4 30. The method of Claim 29, wherein the first  
5 repair process comprises a focused ion beam repair  
6 process, and wherein the second repair process comprises  
7 a laser repair process.

8  
9 31. A system for creating a reticle data file from  
10 an integrated circuit (IC) layout data file, the system  
11 comprising:

12 a processing module, the processing module  
13 being configured to read the IC layout data file,  
14 identify a plurality of specified layout features in  
15 the IC layout data file, and define a halo region  
16 having a substantially constant width around each of  
17 the plurality of specified layout features; and

18 a graphical display, the graphical display  
19 being configured to provide a graphical user  
20 interface (GUI) to allow user input and control of  
21 the processing module.

22  
23 32. The system of Claim 31, wherein the processing  
24 module comprises a personal computer.

25  
26 33. The system of Claim 31, wherein the processing  
27 module is coupled to receive the IC layout data file from  
28 a remote database through a local area network.

29  
30 34. The system of Claim 33, wherein the processing  
31 module is coupled to receive the IC layout data file from  
32 a remote database through a wide area network.

33



1           35. The system of Claim 33, wherein the processing  
2 module is directly connected to a reticle writing tool.

3

4           36. The system of Claim 33, wherein the processing  
5 module is configured to send the reticle data file to a  
6 reticle writing tool through a local area network.

7

8           37. The system of Claim 33, wherein the processing  
9 module is configured to send the reticle data file to a  
10 reticle writing tool through a wide area network.

11

12           38. A reticle for transferring an integrated  
13 circuit layout to a wafer, the reticle comprising:

14           at least one layout feature having an area  
15           designated a tight tolerance feature and an area  
16           designated as a proximity effect halo.

**AMENDED CLAIMS**

[received by the International Bureau on 21 November 2001 (21.11.01);  
original claims 1, 3-4, 7-8, 12-16, 22-24, 26-29; original claims 31-37 cancelled;  
new claims 39-53 added; remaining claims unchanged (11 pages)]

1. (Amended) A method for creating a lithography reticle from an integrated circuit (IC) layout data file, the method comprising:

identifying a plurality of layout features in the IC layout data file;

defining a plurality of halo regions, each of the plurality of halo regions having an inner perimeter and an outer perimeter, the inner perimeter of each of the plurality of halo regions being defined by the outer perimeter of a corresponding one of the plurality of layout features, and the inner perimeter and the outer perimeter of each of the plurality of halo regions being substantially parallel; and

performing an operation using a first set of parameters and a second set of parameters, the first set of parameters being associated with the plurality of critical layout features and the plurality of halo regions, the second set of parameters being associated with the IC layout data file not including the plurality of critical layout features and the plurality of halo regions, the first set of parameters being different from the second set of parameters.

2. The method of Claim 1, wherein each of the plurality of halo regions has a substantially constant width.

3. (Amended) The method of Claim 1, wherein identifying the plurality of critical layout features comprises manually selecting features within the IC layout data file.

4. (Amended) The method of Claim 1, wherein identifying the plurality of critical layout features comprises:

- specifying a layout element;
- scanning the IC layout data file; and
- flagging locations in the IC layout data file matching the layout element.

5. The method of Claim 4, wherein the layout element comprises a transistor gate.

6. The method of Claim 4, wherein the layout element comprises a capacitor.

7. (Amended) The method of Claim 1, wherein identifying the plurality of critical layout features comprises:

- specifying a plurality of layout elements;
- scanning the IC layout data file; and
- flagging locations in the IC layout data file matching one of the plurality of layout elements.

8. (Amended) The method of Claim 1, wherein the IC layout data file comprises a plurality of layer layouts, each of the layer layouts corresponding to a single process layer in a completed IC, wherein identifying the plurality of critical layout features comprises:

- specifying a layout feature configuration;
- scanning a first one of the plurality of layer layouts; and

flagging locations in the first one of the plurality of layer layouts matching the layout feature configuration.

9. The method of Claim 8, wherein the layout feature configuration comprises a single-layer configuration.

10. The method of Claim 8, wherein the layout feature configuration comprises a multi-layer configuration.

11. The method of Claim 10, wherein the first one of the plurality of layer layouts corresponds to a polysilicon layer of the completed IC, and wherein the multi-layer configuration comprises a feature in the first one of the plurality of layer layouts formed over any feature in a second one of the plurality of layer layouts, the second one of the plurality of layer layouts corresponding to a diffusion layer of the completed IC.

12. (Amended) The method of Claim 1, wherein identifying the plurality of critical layout features comprises:

- scanning the IC layout data file;
- identifying optical proximity correction (OPC) features; and
- flagging locations in the IC layout data file associated with the OPC features.

13. (Amended) The method of Claim 2, wherein defining a plurality of halo regions comprises:

defining the inner perimeter of each of the plurality of halo regions;  
specifying a parallel line at the substantially constant width from each edge of the inner perimeter of each of the plurality of halo regions; and  
connecting the parallel lines around each inner perimeter of each of the plurality of halo regions.

14. (Amended) The method of Claim 13, wherein the substantially constant width is defined to be a distance at which proximity effects in a lithography process associated with the IC layout are less than a specified threshold level.

15. (Amended) The method of Claim 13, wherein the substantially constant width is defined to be a distance at which proximity effects in a reticle formation process associated with the IC layout are less than a specified threshold level.

16. (Amended) The method of Claim 13, wherein the substantially constant width is defined to be the greater of a first distance, at which proximity effects in a lithography process associated with the IC layout are less than a specified threshold level, and a second distance, at which proximity effects in a reticle formation process associated with the IC layout are less than the specified threshold level.

17. The method of Claim 14, wherein the distance is determined empirically using measured proximity effect data.

18. The method of Claim 14, wherein the lithography reticle is used in a lithography process using an exposing radiation of a substantially constant wavelength and having a substantially constant numerical aperture (NA), the distance being estimated by dividing the substantially constant wavelength by the NA and multiplying the result by a constant correction factor to compensate for resist and etch effects.

19. The method of Claim 18, wherein the distance is approximately equal to 1.5 microns when the substantially constant wavelength is 365 nm and the NA is 0.6.

20. The method of Claim 18, wherein the distance is approximately equal to 1.0 microns when the substantially constant wavelength is 248 nm and the NA is 0.6.

21. The method of Claim 15, wherein the distance is between  $3.0\mu\text{m}$  and  $3.75\mu\text{m}$  for a 50keV electron beam reticle writing process.

22. (Amended) The method of Claim 1 wherein the operation comprises writing the IC layout data file to a lithography reticle.

23. (Amended) The method of Claim 22, wherein writing the IC layout data file to the lithography reticle is performed using a raster scan tool, the raster scan tool having a first beam spot size and a second beam spot size, the first beam spot size being smaller than the second beam spot size, wherein the

first set of parameters comprises the first beam spot size and the second set of parameters comprises the second beam spot size, and wherein writing the IC layout data file to the lithography reticle comprises:

rastering the portions of the lithography reticle corresponding to the plurality of critical layout features and the plurality of halo regions using the first beam spot size; and

rastering the remainder of the lithography reticle using the second beam spot size.

24. (Amended) The method of Claim 22, wherein writing the IC layout data file to the lithography reticle is performed using a vector scan tool, the vector scan tool being capable of generating an adjustable electron beam, wherein writing the IC layout data file to the lithography reticle comprises:

combining each of the plurality of halo regions with the corresponding one of the plurality of critical layout features to define a plurality of tight tolerance zones;

fracturing each of the plurality of tight tolerance zones into a first plurality of primitives according to the first set of parameters, wherein each of the first plurality of primitives comprising one of a plurality of shapes that can be formed by the adjustable electron beam;

fracturing the remainder of the IC layout data file into a second plurality of primitives according to the second set of parameters, each of the second plurality of primitives comprising one of the plurality of shapes that can be formed by the adjustable electron beam;

exposing each of the first plurality of  
primitives;

and

exposing each of the second plurality of  
primitives.

25. The method of Claim 24, wherein each of the first plurality of primitives has a width greater than a base width, the base width being sized to be larger than the minimum beam width of the vector scan tool.

26. (Amended) The method of Claim 24, wherein a negative resist process is used, and wherein fracturing each of the plurality of tight tolerance zones comprises forming a single primitive around each of the plurality of critical layout features.

27. (Amended) The method of Claim 24, wherein a positive resist process is used, and wherein fracturing each of the plurality of tight tolerance zones comprises forming a set of primitives of substantially similar shape around each of the plurality of critical layout features.

28. (Amended) The method of Claim 22, wherein the operation comprises inspecting a lithography reticle, wherein inspecting the lithography reticle comprises:

inspecting portions of the lithography reticle corresponding to the plurality of halo regions and the plurality of critical layout features according to a first level of scrutiny, wherein the first set of parameters comprises the first level of scrutiny; and



inspecting portions of the lithography reticle not corresponding to the plurality of halo regions and the plurality of critical layout features according to a second level of scrutiny, wherein the second set of parameters comprises the second level of scrutiny, the first level of scrutiny being more rigorous than the second level of scrutiny.

29. (Amended) The method of Claim 22, wherein the operation comprises repairing a lithography reticle, wherein repairing the lithography reticle comprises:

repairing a first plurality of defects within the plurality of halo regions and the plurality of critical layout features using a first repair process, wherein the first set of parameters comprises the first repair process; and

repairing a second plurality of defects not within the plurality of halo regions and the plurality of critical layout features using a second repair process, wherein the second set of parameters comprises the second repair process, the first repair process being more accurate than the second repair process, and the second repair process being faster than the first repair process.

30. The method of Claim 29, wherein the first repair process comprises a focused ion beam repair process, and wherein the second repair process comprises a laser repair process.

(CLAIMS 31 - 37 ARE CANCELLED.)

38. A reticle for transferring an integrated circuit layout to a wafer, the reticle comprising: at least one layout feature having an area designated as a tight tolerance feature and an area designated as a proximity effect halo.

(CLAIMS 39 - 53 ARE NEWLY ADDED)

39. A system for using an IC layout data file, the system comprising:

a processing module configured to read the IC layout data file, identify a plurality of specified layout features in the IC layout data file, and define a halo region around each of the plurality of specified layout features; and

an operating tool configured to perform a first operation associated with the plurality of specified layout features and the halo regions around each of the plurality of specified layout features, and perform a second operation associated with the IC layout data file not including the plurality of specified layout features and the halo regions around each of the plurality of specified layout features, wherein the first operation is different from the second operation.

40. The system of Claim 39, wherein the halo region around each of the plurality of specified layout features comprises a substantially constant width.

41. The system of Claim 40, wherein the substantially constant width is defined to be a distance at which proximity effects in a lithography process

associated with the IC layout data file are less than a specified threshold level.

42. The system of Claim 40, wherein the substantially constant width is defined to be a distance at which proximity effects in a reticle formation process associated with the IC layout data file are less than a specified threshold level.

43. The method of Claim 40, wherein the substantially constant width is defined to be the greater of a first distance, at which proximity effects in a lithography process associated with the IC layout data file are less than a specified threshold level, and a second distance, at which proximity effects in a reticle formation process associated with the IC layout data file are less than the specified threshold level.

44. The system of Claim 39, wherein the plurality of specified layout features comprises a plurality of optical proximity correction features.

45. The system of Claim 39, wherein the processing module further comprises a graphical display, the graphical display being configured to provide a graphical user interface (GUI) to allow user input and control of the processing module.

46. The system of Claim 39, wherein the processing module comprises a personal computer.

47. The system of Claim 39, wherein the processing module is coupled to receive the IC layout data file from a remote database through a local area network.

48. The system of Claim 39, wherein the processing module is coupled to receive the IC layout data file from a remote database through a wide area network.

49. The system of Claim 39, wherein the operating tool comprises a reticle writing tool.

50. The system of Claim 49, wherein the processing module is configured to send a reticle data file to the reticle writing tool through a local area network.

51. The system of Claim 49, wherein the processing module is configured to send a reticle data file to the reticle writing tool through a wide area network.

52. The system of Claim 39, wherein the operating tool comprises a reticle inspection tool.

53. The system of Claim 39, wherein the operating tool comprises a reticle repair tool.

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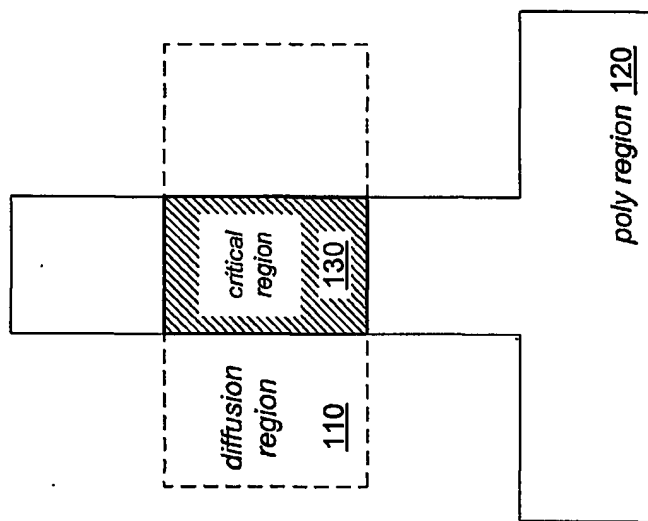


Fig. 1  
(PRIOR ART)

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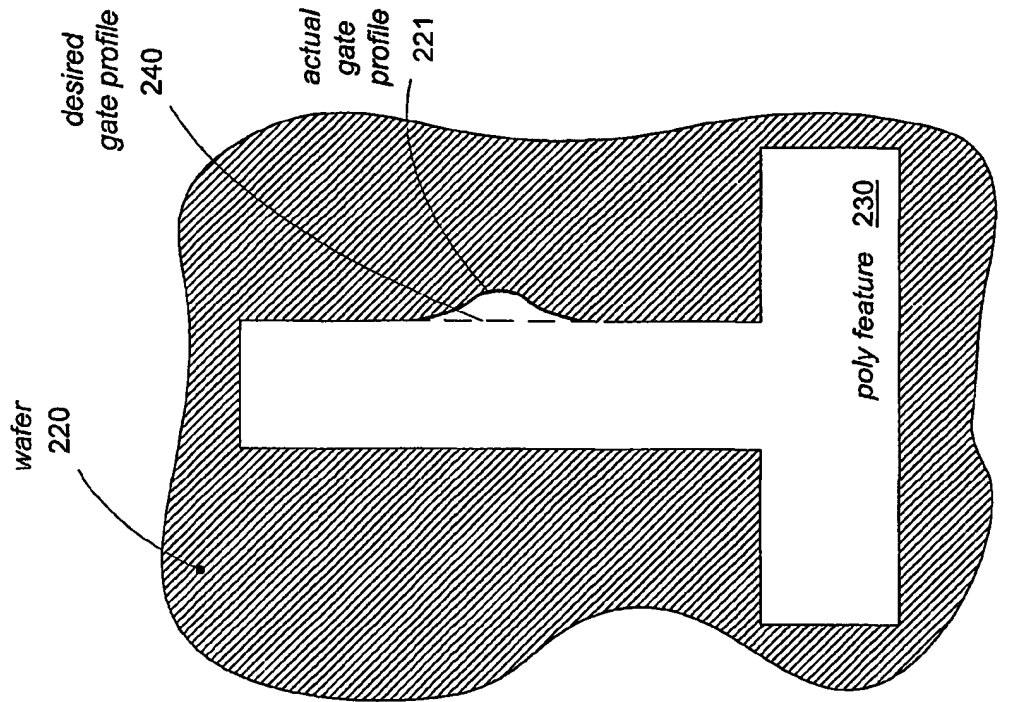


Fig. 2b

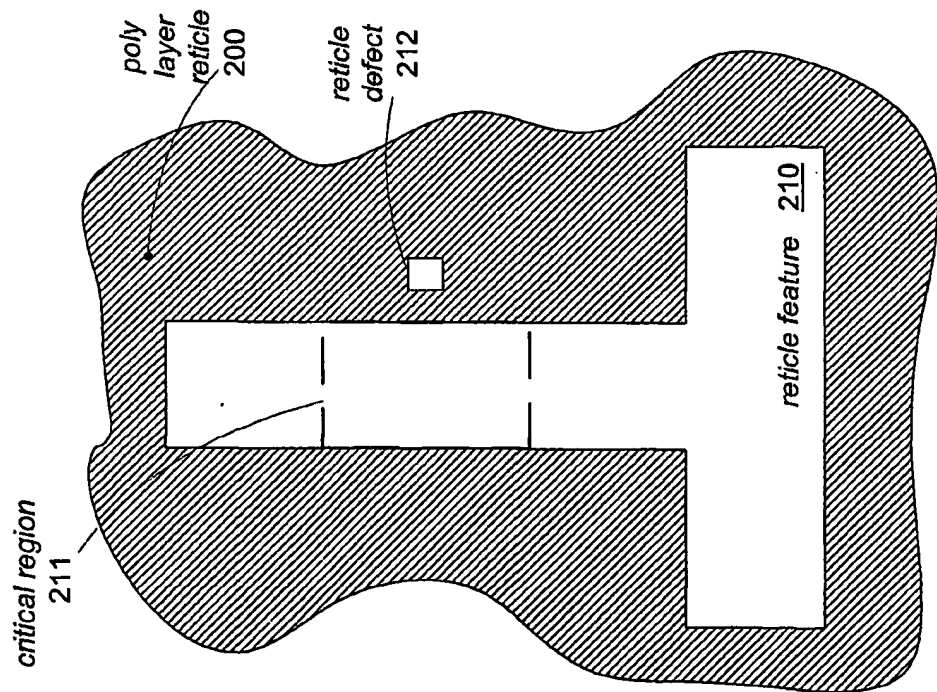


Fig. 2a

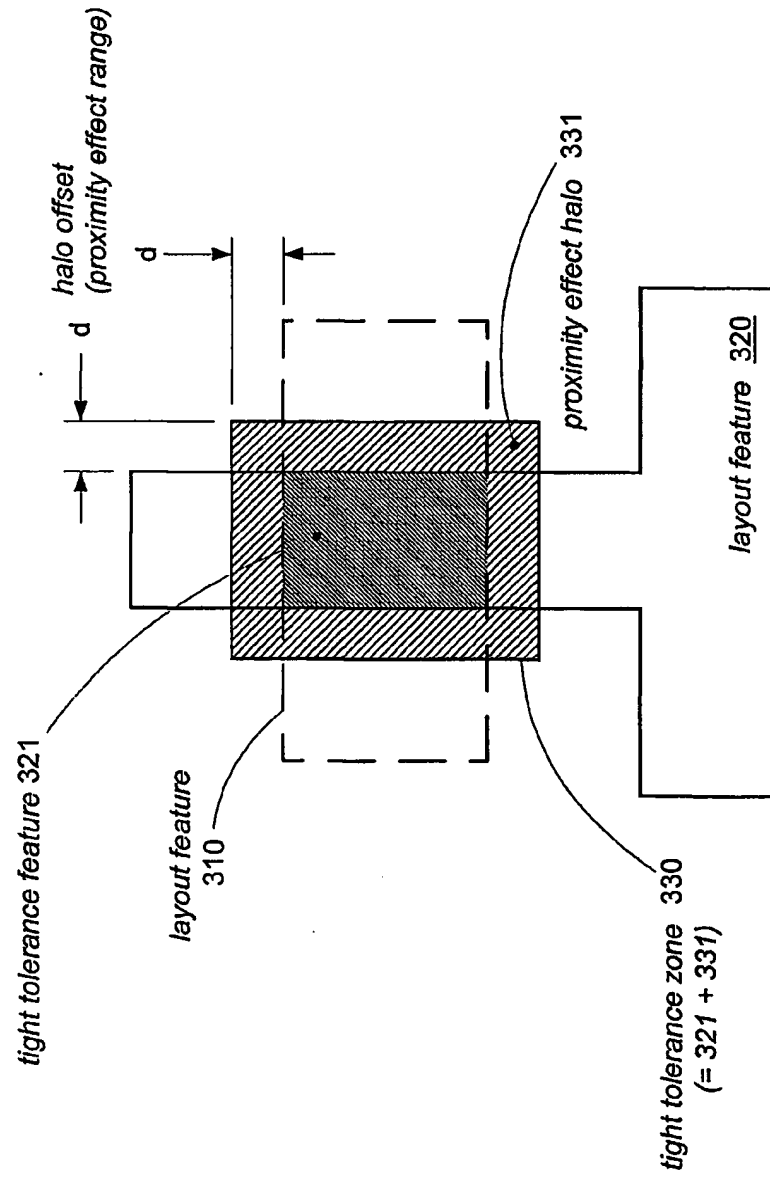


Fig. 3

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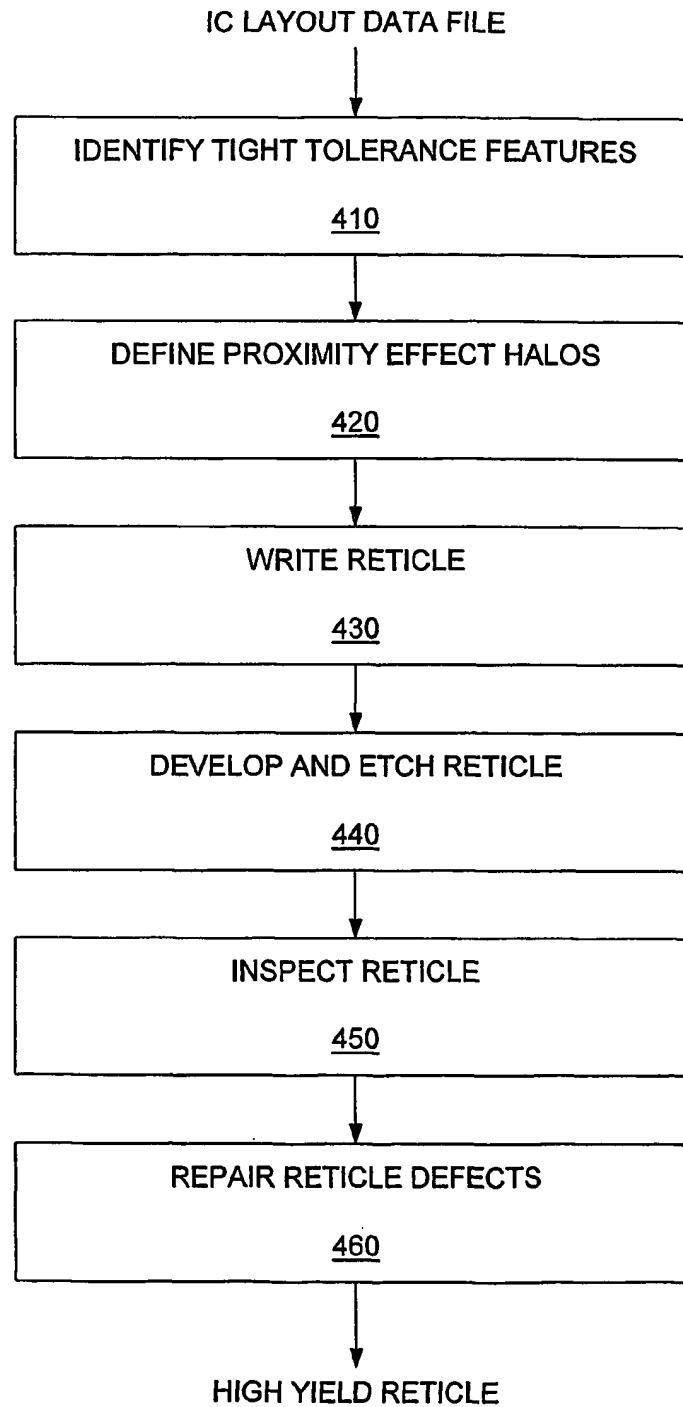


Fig. 4a



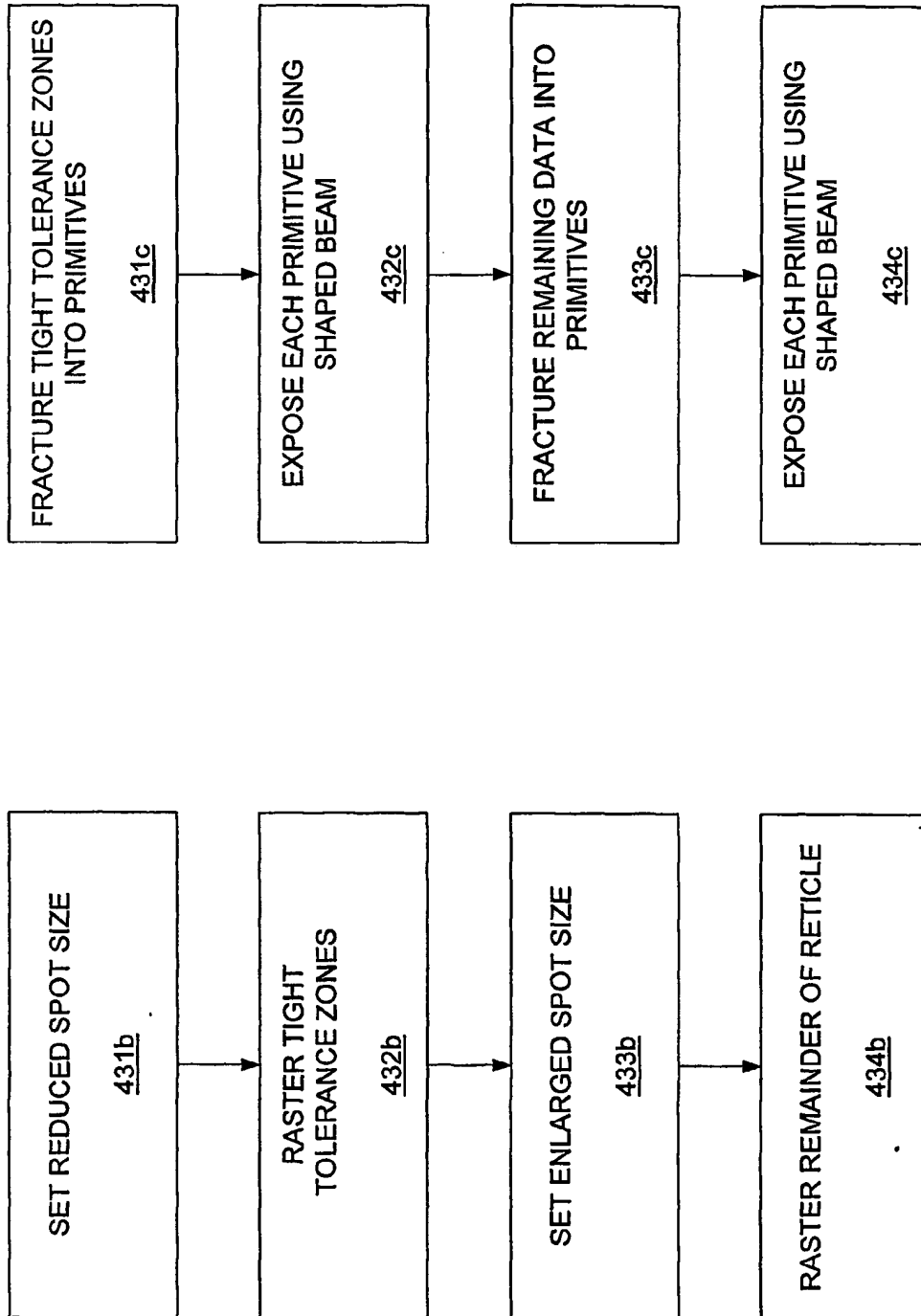


Fig. 4b

Fig. 4c

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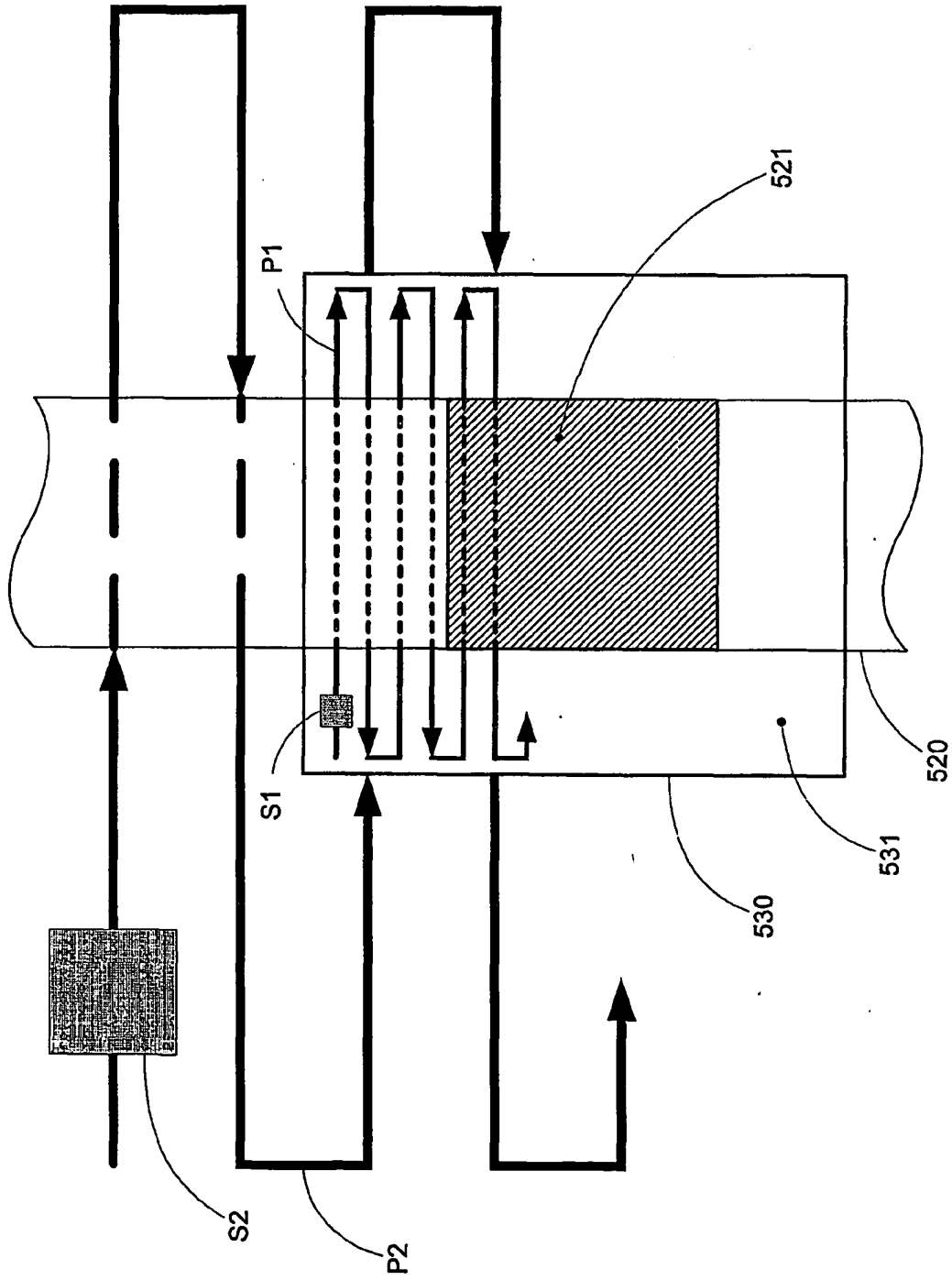


Fig. 5

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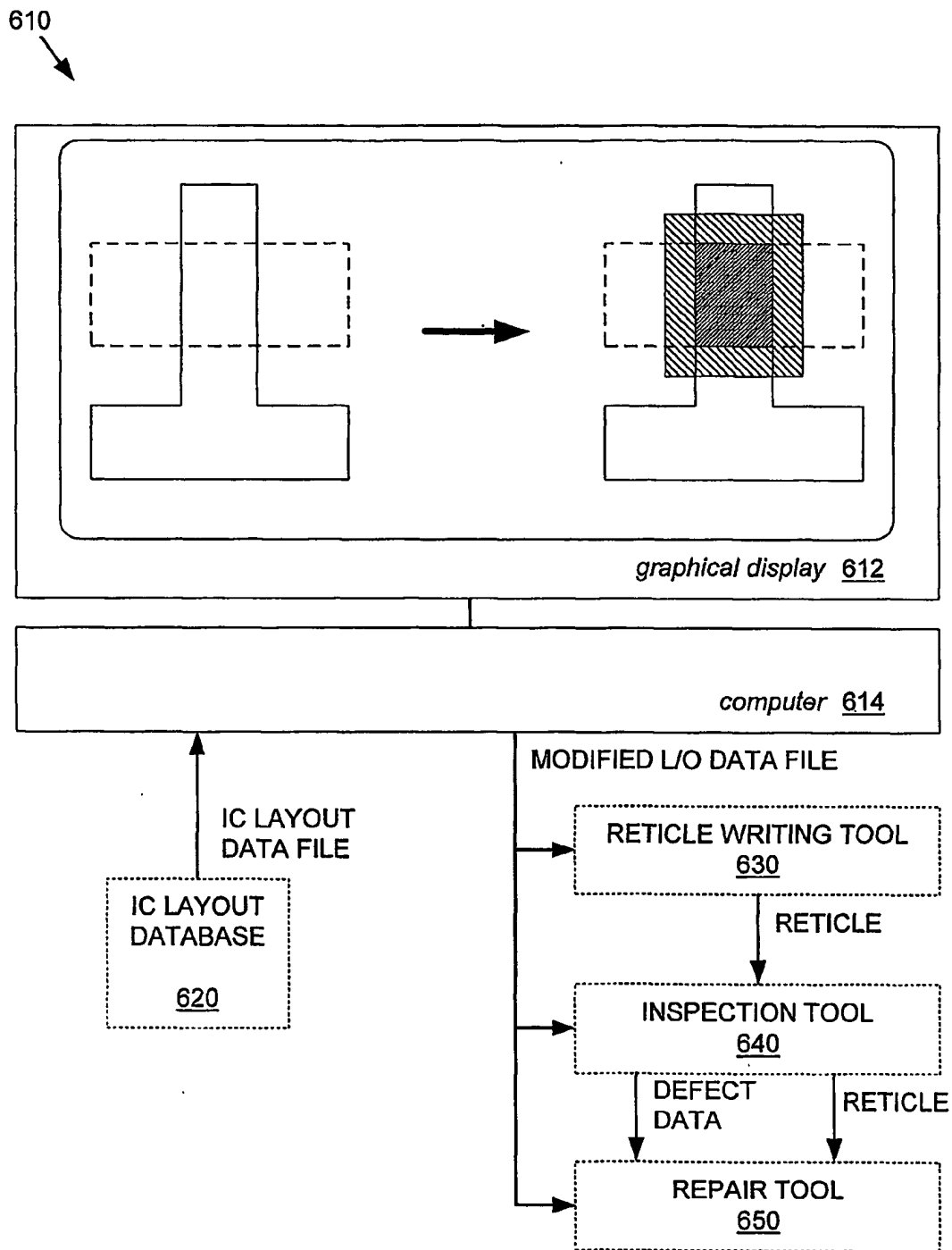


Fig. 6

## INTERNATIONAL SEARCH REPORT

Inventor's Application No  
PCT/US 00/35653

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 G03F1/14 G03F7/20 H01J37/302

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 G03F H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, IBM-TDB, COMPENDEX, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 344 436 A (NIPPON ELECTRIC CO) 7 June 2000 (2000-06-07) the whole document	1-8, 10-38
X	US 4 895 780 A (NISSAN-COHEN YOAV ET AL) 23 January 1990 (1990-01-23) the whole document	1-9, 11-38
A	WO 00 36525 A (KLA TENCOR CORP) 22 June 2000 (2000-06-22)	
A	US 4 692 579 A (SAITOU NORIO ET AL) 8 September 1987 (1987-09-08)	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the International search

21 September 2001

Date of mailing of the International search report

01/10/2001

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# INTERNATIONAL SEARCH REPORT

Information on parent family members

Int. Application No

PCT/US 00/35653

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
GB 2344436	A	07-06-2000	JP 2000147744 A CN 1254180 A US 6174633 B1	26-05-2000 24-05-2000 16-01-2001
US 4895780	A	23-01-1990	NONE	
WO 0036525	A	22-06-2000	WO 0036525 A2	22-06-2000
US 4692579	A	08-09-1987	JP 60244026 A JP 2003350 C JP 7032110 B JP 60244024 A JP 2012869 C JP 7027854 B JP 60244025 A	03-12-1985 20-12-1995 10-04-1995 03-12-1985 02-02-1996 29-03-1995 03-12-1985